SRIC/06

INDIAN INSTITUTE OF TECHNOLOGY, ROORKEE
(Department of Electronics and Communication Engineering)

Dated: 20.08.2026

ADVERTISEMENT TO FILL UP PROJECT POSITION

Applications are invited from Indian nationals only for project position as per the details given below for the consultancy/research project under the **Principal investigator (Prof. Anand Bulusu)**, Department of Electronics and Communication Engineering, Indian Institute of Technology, Roorkee.

1. **Title of project- "GF University Centre"**
2. **Sponsor of the project- Global Foundries**
3. **Project position and number- Junior Research Fellow (JRF)- 01**
4. **Qualifications- B.Tech./ B.E. in Electronics and Communication Engineering/ Materials Science Engineering / Materials Engineering/ Electrical Engineering/ Electrical and Electronics Engineering/ Physics Engineering /Applied Physics Engineering (min CGPA 7.0/10 or 70%) and a valid GATE scorecard**
5. **Emoluments- Rs. 37,000/- + HRA (as per norms)**
6. **Duration- 1 Year from the date of joining**
7. **Job description- Knowledge of semiconductor devices, RRAM/emerging memories, VLSI, device fabrication, neuromorphic computing, SNNs, or Python/MATLAB, data analysis**

1. Candidates before appearing for the interview shall ensure that they are eligible for the position they intend to apply.
2. Candidates desiring to appear for the Interview should submit their applications by 07 September 2026 with the following documents via email to **vlsi-office@ece.iitr.ac.in**:
   - Application in a plain paper with detailed CV including chronological discipline of degree/certificates obtained.
   - Experience including research, industrial field and others.
   - Attested copies of degree/certificate and experience certificate.
3. Candidate shall bring along with them the original degree(s)/certificate(s) and experience certificate(s) at the time of interview for verification.
4. Preference will be given to SC/ST candidates on equal qualifications and experience.
5. Please note that no TA/DA is admissible for attending the interview.

Note: The selected candidate may get an opportunity for PhD/ MS by Research.
The last date for receiving the applications is ~~07 September 2026~~ 16 September 2026. The date of Interview shall be intimated to the shortlisted candidates only through email.

APPROVED

B. Anand

Dean
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Indian Institute of Technology Roorkee
Roorkee-247 667 (INDIA)
21/08/2026

21/8/26

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Name and signature of Principal Investigator

*To be uploaded on the IIT Roorkee website, and a copy may be sent to the appropriate addresses by the PI for wider circulation.

Job description:

This project focuses on the design, optimization, and characterization of low-voltage Logic and SRAM IPs for ultra-low-power SoCs, targeting 0.45-V retention and always-on operation. Key activities include standard-cell library development, SRAM/memory-cell characterization methodology, timing/power/energy modeling, and PVT and process-variation-aware analysis. The work involves circuit simulation, library characterization, synthesis, STA, and power analysis using EDA tools. This also requires expertise in programming skills including Python/MATLAB. The project also explores near-/sub-threshold CMOS circuit design, with opportunities for PhD or MS by research and industry-based internships in collaboration with GlobalFoundries.

Scope:

The project focuses on the development of energy-efficient low-voltage Logic and SRAM IPs for next-generation ultra-low-power SoCs. The work encompasses standard-cell library design and characterization, SRAM/memory-cell characterization and methodology development, and optimization of always-on logic and 32-kHz RTC wake-up circuits at a 0.45-V retention supply. The project targets significant SoC power reduction through robust operation across low-voltage voltage regime, incorporating PVT/variability analysis, semiconductor-device understanding, VLSI and emerging-memory technologies, and EDA-based characterization.

Opportunities:

1. PhD/MS by Research: Opportunity to pursue a research degree while working on industry-relevant low-voltage Logic and SRAM IP development.
2. Industry Internship: Opportunity for an industry-based internship during the course of the project through close collaboration with GlobalFoundries (GF).
3. Industry Exposure: Gain hands-on exposure to advanced semiconductor technologies, EDA-based design and characterization methodologies, and industry-oriented IP development.
4. Research & Innovation: Opportunity to contribute to research in ultra-low-power VLSI, SRAM/emerging memories, always-on computing, and near-/sub-threshold circuit design.
5. Publications & Technology Development: Scope for research publications, technology demonstrations, and development of practical low-power semiconductor IPs.

Responsibilities:

1. Design and characterize low-voltage standard cells for operation at 0.45 V, targeting minimum power and energy with reliable timing.
2. Develop characterization methodologies and techniques for standard cells and SRAM/memory cells across PVT and process variations.
3. Develop and validate timing, power, energy, and leakage models for low-voltage logic and memory IPs.
4. Analyze and optimize Always-On logic and 32-kHz RTC wake-up circuits operating from the 0.45-V retention rail.
5. Perform EDA-based circuit simulation, library characterization, synthesis, STA, and power analysis to validate the developed IPs.
6. Contribute to research publications, technical reports, IP development, and industry-oriented technology validation in collaboration with academic and GlobalFoundries teams.