



INDIAN INSTITUTE OF TECHNOLOGY GANDHINAGAR

Research & Development Office

ADVERTISEMENT NO. SPON/62034/Advt0316 DATED 14.09.2026

Applications are invited for a temporary position of **Junior Research Fellow** at IIT Gandhinagar. The details are as below:

Name of PI	Prof. Joycee Mekie	Department	Electrical Engineering
Project title	Secure and Energy efficient Mixed domain Compute in memory-based AI accelerator Chip for Edge applications		
Designation	Junior Research Fellow		
Number of positions	02		
Application Link	http://recruitment.iitgn.ac.in/projectstaff/		
Last date of application submission	25.09.2026		
Consolidated Monthly Remuneration including HRA	₹ 45,880/- per month		
House Rent Allowance per month (If applicable)	₹ 8,880 payable as per Institute norms		
Duration of appointment	1 year		
Eligibility Norms ¹	☐ Institute norms ☒ Funding Agency norms		
Essential Qualification/Experience as per the norms ¹	Post Graduate Degree in Basic Science OR Graduate / Post Graduate Degree in Professional Course selected through a process described through any one of the following a)Scholars who are selected through NET, CSIR-UGC NET including lectureship (Assistant Professorship) and GATE. b)The selection process through National level examinations conducted by Central Government Departments and their Agencies and Institutions such as DST, DBT, DAE, DOS,DRDO, MoE, ICAR, ICMR, IIT, IISc,IISER, NISER etc. <i>The percentage/grade points with respect to the academic qualification will be a minimum 60% or equivalent grade from graduation onwards and 55% or equivalent grade in class 10th and 12th.</i>		
Desirable Qualification/Experience	BTech / BE / MTech / ME degree in Electrical/Electronics/Electronics and Communications / Electronics and Instrumentation/Computer Science and Engineering/Computer Science or related disciplines with at least 60% or equivalent. The candidates with experience of using VLSI EDA tools will be preferred and those with decent coding skills will be preferred. Candidates with excellent programming skills C/C++/Python, Verilog/System Verilog or equivalent, etc. and candidates with interest in computer architecture and having knowledge of system simulators will be given preference. Students with exposure of Analog Circuits, ADCs, DACs, etc. and experience with Chip design will be preferable.		



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Job Description	Applications are invited for 02 JRF position for MEITY sponsored project in C2S. The candidate is expected to have excellent understanding of Digital & Analog Circuits, VLSI design, etc. and should have a exposure to relevant VLSI tools and techniques.
Contact	Prof. Joycee Mekie, Professor, Department of Electrical Engineering, Email: joycee@iitgn.ac.in

“Merely meeting the minimum eligibility criteria will not guarantee the shortlisting and/or appointment. A higher cutoff level may be used. The Institute reserves all rights, not to call an applicant for a selection test or not to fill up a position through this round of selection process without assigning any reason.”